the frame buffer.

13–2. CHRP platforms must minimally support a 640x480 linear frame buffer with the Open Firmware characteristics and interfaces described in the CHRP Linear Frame Buffer Device Binding.

13–3. VGA compatibility is optional; if VGA compatibility is provided, it must adhere to the programming model given in Appendix A, “VGA Programming Model,” on page 195.

13–4. If VGA compatibility is provided, it must conform with the characteristics and interfaces described in the CHRP VGA Display Device Binding.

13–5. If VGA compatibility is provided, the display node of the Open Firmware device tree must indicate a compatible property of “pnpPNP,900”. Conversely, if the compatibility property of “pnpPNP,900” is indicated in the display node of the Open Firmware device tree, the programming model described in Appendix A, “VGA Programming Model,” on page 195 must be present.

Chapter 14 Versatile Interface Adapter (VIA)

14–1. The Open Firmware device tree node for the device described in this chapter must follow the specifications given in the Mac I/O [14] Open Firmware device binding.

14–2. The Open Firmware “reg” property information given in Table 311 on page 167 must be provided in the Open Firmware device tree for the VIA device.

14–3. New capabilities in operating systems must not depend in any way on the continued existence of the facilities described in the VIA chapter.

14–4. New software must not utilize the timing characteristics associated with operations on the VIA hardware as described in Section 14.3.2, “Internal Timings,” on page 166 of the VIA chapter.

14–5. All the “reg” property fields specified in Table 311 on page 167, “VIA Registers”, must comply with the format given in the PCI binding to IEEE Std 1275-1994, as modified by the CHRP binding to IEEE Std 1275-1994.

14–6. Software must not write to the Peripheral Control Register in the VIA hardware.

Chapter 15 Descriptor-Based DMA

15–1. Every DBDMA reserved field must be 0 when written and must be ignored when read. This must be true whether the reserved field is accessed by the DBDMA hardware or by device driver software.

15–2. Some address pointers are constrained to be multiples of 4, 8, or 16 bytes. For example, the NewCommandPtr value is always 16-byte aligned. The least-significant bits of these aligned addresses must be reserved, to ensure deterministic behavior when unaligned address values are used.

15–3. The PCI devices described herein are allowed one interrupt each to the system. DBDMA interrupts must be shared with the other interrupt requirements of the device as described in the device chapters.

Glossary

This glossary contains an alphabetical list of terms, phrases, and abbreviations used in this document.

Term	Definition
µs	Microsecond or one millionth of a second
ACD	Active device register
ADB	Apple Desktop Bus
ADC	Analog-to-digital converter
ADDR	Address register
AEJ	Autoeject register
AFIFO	Address first in - first out register
A/N	Alphanumeric
ANSI	American National Standards Institute
APA	All points addressable
Architecture	The hardware/software interface definition or software module to software module interface definition.
ASCII	American National Standards Code for Information Interchange
BA	Base address register
BC	Base count register
BE	Big Endian
BIOS	Basic input/output system
BLOP	Base low page register
CA	Current address register
CBP	Clear byte pointer register
CC	Current count register
CCR	Configuration control register
CDRF	Command/data register file

CHIP	Current high page register
CHRP	Common Hardware Reference Platform
CLOP	Current low page register
CMD	Command register
CRT	Cathode ray tube which normally refers to a computer monitor
CTL	Control register
CTR	Control register
DAC	Digital-to-analog converter
DAT	Data register
DATA	EPP data port register
DATAR	Data register
DBDMA	Descriptor based direct memory access
DCM	DMA channel mode register or DMA clear mark register
DCEM	DMA extended mode register
DCOM	DMA command register
DCR	Control register
DET	Detect register
DFIFO	Data first in - first out register
DIR	Digital input register
DLH	Baud rate divisor high order register
DLL	Baud rate divisor low order register
DMA	Direct memory access
DMC	DMA master clear register
DOR	Digital Output Register
DR	DMA request register
DRS	Data rate select register
DS	DMA status register
DSR	Status register
DTC	Data type count register
DTR	Data register
ECP	Extended capability parallel port
ECR	Extended control register
EDR	Extended data register

EIR	Extended index register
ELI	Edge level interrupt control register
ENH	Enhanced register
EOL	End of line
EPP	Enhanced parallel port
ESR	Error status register
ESSC	Extended serial communications controller
FCR	First in - first out control register
FIFO	First in - first out or bus first in - first out register
FifoCount	FIFO count register
GB	Gigabytes - as used in this document it is 2 raised to the power of 30
Hz	Hertz
ICW	Initialization control word
ID	Identification
IDE	Integrated device electronics
IEEE	Institute of Electrical and Electronics Engineers
IER	Interrupt enable register
IIR	Interrupt identification register
I/O	Input/output
IN	Input register
IrDA	Infrared Data association which sets standards for infrared support including protocols for data interchange
IRQ	Interrupt request
IRR	Interrupt request register
ISA	Industry standard architecture (typically refers to the PC local bus)
ISE	Interrupt source enable register
ISO	International Organization of Standards
ISR	In-service register
IST	Interrupt status register
KB	Kilobytes - as used in this document it is 2 raised to the power of 10
KHz	Kilo Hertz
LCD	Liquid crystal display
LCR	Line control register
LE	Little Endian

LFB	Linear frame buffer
lsb	Least significant bit
LSR	Line status register
LTPC	LocalTalk protocol controller
MCR	Modem control register
MSR	Main status register or Modem status register
MB	Megabytes - as used in this document it is 2 raised to the power of 20
MESH	Macintosh enhanced SCSI hardware
MeshFeature	MESH features register
MeshID	MESH identification register
ms	Milliseconds or thousandths of a second
N/A	Not applicable
ns	Nanoseconds or billionths of a second
OCW	Operation control word
OF	Open Firmware
OS	Operating system
OUT	Output register
PC	Personal computer
PC Card	A memory or I/O card compatible with the *PC Card Standard* []. When cards are referred to as PC Cards, what is being addressed are those characteristics common to both 16-bit PC Cards and CardBus PC Cards.
PCI	Peripheral Component Interconnect
PCMCIA	Personal Computer Memory Card International Association (see PC Card)
PCR	Primary command register
PEL	Picture element
PIC	Programmable interrupt controller
Platform	Refers to the hardware plus firmware portion of a system composed of hardware, firmware, and operating system.
PPRD	Primary PRD table address register
PRD	Physical region descriptor
PSR	Primary status register
RAM	Random access memory
RC	Recovery count register
RDR	Receiver data register

Reserved	The term “reserved” is used within this document to refer to bits in registers or areas in address spaces which should not be referenced by software except as described in this document. Normally when writing other bits in a register with reserved bits, the register should be read, the non reserved bits set, and the register should be written.
RMSK	Receive mask register
ROM	Read only memory
SCC	Serial communications controller
SCDR	Special character detect register
SCR	Scratch control register or secondary command register
SCSI	Small computer system interface
SelTO	Selection time out register
SGC	Scatter/gather command register
SGD	Scatter gather descriptor
SGIS	Scatter/gather interrupt status register
SGPTR	Scatter/gather descriptor table pointer register
SGS	Scatter/gather status register
SP	Special character register
SPP	Standard parallel port
SPRD	Secondary PRD table address register
SR	Status register
SRQ	Service request
SSR	Secondary status register
ST	Status register
STA	Status register
STR	Status register
STRT	Start register
SyncParms	Synchronous parameters register
System	Refers to the collection of hardware, system firmware, and operating system software which comprise a computer model.
System firmware	Refers to the collection of all firmware on a system including Open Firmware, RTAS, and any legacy firmware.
System software	Refers to the combination of operating system software, device driver software, and any hardware abstraction software, but excludes the application software.
TC	Terminal count register

TDR	Table drive register or Transmitter data register
TMR	Timer register
UART	Universal asynchronous receiver/transmitter
VESA	Video Electronics Standards Association
VGA	Video graphics array
VIA	Versatile interface adapter
WAM	Write all mask bits register
WSM	Write single bit mask register
x86	Intel processors such as 80386, 80486,...
XferCount	Transfer count register

Trademark Information

The following terms, denoted by a registration symbol (®) or trademark symbol (™) on the first occurrence in this publication, are registered trademarks or trademarks of the companies as shown in the list below:

Trademark	Company
Apple Desktop Bus	Apple Computer, Inc.
AIX	International Business Machines Corporation
Apple	Apple Computer, Inc.
CHRP	Apple Computer, Inc.
Ethernet	Xerox
GeoPort	Apple Computer, Inc.
IBM	International Business Machines Corporation
LocalTalk	Apple Computer, Inc.
Macintosh	Apple Computer, Inc.
Mac	Apple Computer, Inc.
Motorola	Motorola, Inc.
PowerPC	International Business Machines Corporation
PS/2	International Business Machines Corporation
Solaris	SunSoft
Windows	Microsoft Corporation
Windows NT	Microsoft Corporation

Bibliography

This section lists documents which were referenced in this specification or which provide additional information. Following this list are two sections. The first section gives useful information for obtaining these documents. The second section lists contacts and sources for additional helpful information. The documents are listed below:

1. *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture*, Morgan Kaufmann Publishers, Inc., San Francisco, CA, ISBN 1-55860-394-8
2. *The PowerPC Architecture: A Specification for a New Family of RISC Processors,* Second Edition, Morgan Kaufmann Publishers, Inc., San Francisco, CA, ISBN 1-55860-316-6
3. *Computer Architecture: A Quantitative Approach,* Second Edition Morgan Kaufmann Publishers, Inc., San Francisco, CA, ISBN 1-55860-329-8
4. *PowerPC 603 RISC Microprocessor User's Manual*, IBM order number MPR603UMU-01, Motorola order number MPC603UM/AD
5. *PowerPC 603 RISC Microprocessor Technical Summary*, Rev 3 IBM order number MPR603TSU-03, Motorola order number MPC603/D
6. *PowerPC 604 RISC Microprocessor User's Manual*, IBM order number MPR604UMU-01, Motorola order number MPC604UM/AD
7. *PowerPC 604 RISC Microprocessor Technical Summary*, Rev 1 IBM order number MPR604TSU-02, Motorola order number MPC604/D
8. *Technical Introduction to the Macintosh Family*, Second Edition, Addison-Wesley Publishing Company, Reading, MA, ISBN 0-201-62215-7
9. IEEE 1275, *IEEE Standard for Boot (Initialization Configuration) Firmware, Core Requirements and Practices,* IEEE part number DS02683, ISBN 1-55937-426-8
10. *PCI Local Bus Specification*, Revision 2.1
11. *PowerPC Microprocessor Common Hardware Reference Platform: I/O Device Reference,* available at various electronic sites
12. *PowerPC Reference Platform Specification*, Version 1.1
13. *ANSI X3.131-199x Rev.10L,1992 (SCSI-2): Information Technology - Small Computer System Interface*
14. *Mac I/O* binding for Open Firmware
15. *CHRP ISA Bus Binding to: IEEE Standard 1275-1994*
16. *CHRP ISA Floppy Device Bindingto: IEEE Standard 1275-1994*

17. *Inside Macintosh: Devices*

18. *Macintosh Technology in the Common Hardware Reference Platform*, Morgan Kaufmann Publishers, Inc., San Francisco, CA, ISBN 1-55860-393-X

19. *ADB-The Untold Story* available at http://dev.info.apple.com/technotes/Archive/Hardware/hw_01.html

20. *Intel 82378ZB System I/O (SIO) Specification*

21. *SL82C565 System I/O Controller With PCI Arbiter*, from Winbond Systems Laboratory

22. *CHRP ISA DMA Controller Device Binding to IEEE 1275-1994 Standard for Boot (Initialization, Configuration) Firmware*

23. *CHRP ISA Parallel Port Device Binding to: IEEE 1275-1994 Standard for Boot (Initialization, Configuration) Firmware*

24. *National Semiconductor PC87308VUL SuperI/O™ Enhanced Sidewinder Lite Plug and Play Compatible Chip, with a Floppy Disk Controller, a Keyboard Controller, a Real-Time Clock, Two UARTs, Full Infrared Support and an IEEE1284 Parallel Port*

25. *IEEE Standard Signaling Method for a Bidirectional Parallel Peripheral Interface for Personal Computers*, also called *IEEE Std 1284-1994 Specification*

26. *National Semiconductor PC87332VLJ (3.3V/5V) and PC87332VLJ-5 (5V) (Super I/O III Premium Green) with a Floppy Disk Controller, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface*

27. *IEEE Std 1275-1994, IEEE Standard for Boot (Initialization Configuration) Firmware: Core Requirements and Practices,* published by IEEE.

28. *CHRP ISA Serial Port Device Binding to: IEEE 1275-1994 Standard for Boot (Initialization, Configuration) Firmware*

29. *ANSI ATA Specification Revision 3.2*

30. *ANSI ATAPI Specification (Current Revision?)*

31. *SFF IDE PCI Bus Master Specification??*

32. *PCI Sign IDE PCI Bus Master Specification??*

33. *Open Firmware Bindings for SCSI devices/bus????*

34. *Open Firmware Recommended Practice: 8-bit Graphics Extension,* published by the Open Firmware Working Group

35. *Open Firmware Recommended Practice: 16-color Text Extension,* published by the Open Firmware Working Group

36. *CHRP Linear Frame Buffer Display Device Binding to: IEEE 1275-1994 Standard for Boot (Initialization, Configuration) Firmware*

37. *CHRP VGA Display Device Binding to: IEEE 1275-1994 Standard for Boot (Initialization, Configuration) Firmware*

38. *Personal Computer Standard V2.0 (SurePath BIOS)*

39. *Zilog Serial Communications Controllers: Product Specifications Data Book* Document number: DC8316-01

Sources for Documents

This section provides useful information for obtaining the documents listed above.

The manuals for the PowerPC microprocessors or the *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture* are available from the following sources:

- IBM at 1-800-PowerPC (1-800-769-3772) in the U.S.A
  - If the 1-800-PowerPC number can not be reached or if multilingual operators are required, use 1-708-296-6767
- IBM at (39)-39-600-4455 in Europe
- Motorola at 1-800-845-MOTO (6686)

The *PowerPC Reference Platform Specification* in PostScript format is available via anonymous FTP at ftp://ftp.austin.ibm.com/pub/technology/spec and on CompuServe in the library of the PowerPC forum. The FTP server contains a README file which list the information at this directory.

The *PowerPC Reference Platform Specification* and *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture* are available in Europe electronically from a bulletin board service (BBS). The BBS may be reached at +39-39-600-5076 and supports up to 28.8 KBPS.

The documents published by Morgan Kaufmann Publishers may be purchased in bookstores and may be ordered from Morgan Kaufmann at 1-800-745-7323 or through their home page at http://www.mkp.com. The PowerPC versions may be available from IBM publications sources at 1-800-426-6477 in the US only. In other countries, order from your local source for IBM literature.

PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture is available in html format from http://www.austin.ibm.com/tech/chrp/chrp_book.htlm and in Acrobat viewable PDF format from http://chrp.apple.com.

The approved Open Firmware bindings including *Open Firmware Recommended Practice: 16-color Text Extension* and *Open Firmware Recommended Practice: 8-bit Graphics Extension* are available via anonymous FTP to ftp://playground.sun.com/pub/p1275/bindings/postscript/*.ps.

Call 1-212-642-4900 for orders or inquiries pertaining to ANSI and ISO standards.

To order copies of EIA standards, contact Global Engineering Documents at 1-800-854-7179.

Copies of IEEE standards may be obtained by calling 1-800-678-IEEE. For information about IEEE standards, call 908-562-3800.

To purchase PCI documents, call 1-800-433-5177 in the U.S.A. or 1-503-797-4207 outside the U.S.A.

Copies of PCMCIA standards including the *PC Card Standard* may be obtained by calling PCMIA at 1-408-720-0107 or Fax to 1-408-720-9416 or by calling JEIDA at +81-3-3433-1923 or Fax to +81-3-3433-6350.

Plug and Play information is available on CompuServe Plug and Play forum (GO PLUGPLAY).

Obtaining Additional Information

Several sources exist for obtaining additional information about the PowerPC microprocessor and the *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture*.

Hardware system vendors may obtain information on IBM components or the IBM design kits which give further information on their reference implementation by contacting IBM at the following numbers:

- IBM at 1-800-PowerPC (1-800-769-3772) in the U.S.A
- Within Europe (49)-511-516-3444 in English
- Within Europe (49)-511-516-3555 in German
- In Asia (81)-775-87-4745 in Japanese

Updates to the *The PowerPC Architecture: A Specification for a New Family of RISC Processors* are available at http://www.austin.ibm.com/tech/ppc-chg.html.

The curernt version and updates to *The PowerPC Microprocessor Common Hardware Reference Processor: A System Architecture* and *PowerPC Microprocessor Common Hardware Reference Platform: I/O Device Reference* are available via anonymous FTP from ftp://ftp.austin.ibm.com/pub/technology/spec/chrp.

OEMs, IHVs, and ISVs may obtain information on Motorola products and Motorola system design kits by contacting their local Motorola sales office or 1-800-845-MOTO (6686).

Information on the full range of Motorola's semiconductor, software, design kits, and system products may be found at Motorola's PowerPC World Wide Web home page located at http://www.mot.com/PowerPC/.

Information on the full range of IBM products may be found at IBM's World Wide Web home page located at http://www.ibm.com/.

Information on the full range of Apple products may be found at Apple's World Wide Web home page located at http://www.apple.com/.

An electronic forum on CompuServe has been established for the discussion of PowerPC reference platform topics and for obtaining answers to questions on the PowerPC reference platform. Go to the "PowerPC" forum on CompuServe and join the "Reference Platform" topic.

Information on IrDA documents is available on the World Wide Web at ftp://hplose.hpl.hp.com.

VESA documents including the DDC 1 standard are available on the World Wide Web at http://www.vesa.org.

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